REMARKS/ARGUMENTS

The Office Action mailed April 30, 2007 has been carefully considered. Reconsideration in view of the following remarks is respectfully requested.

The 35 U.S.C. § 102 Rejection

Claims 1-3 were rejected under 35 U.S.C. § 102(b) as being allegedly anticipated by Leeds et al.[1] This rejection is respectfully traversed. Applicants respectfully submit that claim 1 is not anticipated or rendered obvious by Leeds. Claim 1 includes the following limitations.

> Component with a dynamically reconfigurable architecture for processing data comprising a data processing block TD and a general controller CG capable of controlling the data processing block TD characterized in that:
>
> - the block TD comprises a plurality of reconfigurable elementary data processing blocks BE; each elementary block BE comprises two inputs, E1 and E2 for reception of data to be processed, and one output S for transmission of processed data; a common input data bus being capable of transmitting data to be processed to the input E1 of each of the blocks BE and the controller CG; for each block BE, an output data bus connected to its output S, being capable of transmitting processed data outside the component and through a bypass data bus to the input E2 of a single other block BE;
> - the controller CG is capable of initializing configurations of blocks BE and controlling their dynamic reconfiguration, controlling data flows at the output from each block BE so as to transmit data either towards the outside or to the input E2 of another block BE, and controlling data flows at the input of each block BE.

(Claim 1) (Emphasis added)

Applicants respectfully submit that Leeds does not disclose the limitation of a data processing block (a TD block) as claimed, the limitation of a controller (a general controller, CG), as claimed, or the limitation of the output of each elementary block (BE block) being connected to the input of another elementary block.

[1] U.S. Patent No. 5,760,607 to Leeds et al.

Leeds does not disclose a controller capable of initializing configuration and controlling dynamic reconfiguration. The memory circuit 30 is not disclosed as providing a dynamic reconfiguration process.

Moreover, elements 37a, 37b, and 37c cannot be equated with the elementary blocks as claimed. However, even if they were, the outputs of each element 37a, 37b, and 37c is not connected to the input of another elementary block as claimed. The Examiner cites Figure 8a, but a thorough reading of the text describing Figure 8a makes clear that it is not the output of each block that is being connected to the input of another block. In reference to Figure 8a, Leeds discloses the following.

> FIG. 8a illustrates a variation of the embodiment of FIG. 5a, in which three FPGAs 37a, 37b and 37c are configured. All three devices receive the clock signal from memory 30 via lead 35. Of importance, FPGAs 37a and 37b include serial output leads 76a and 76b, respectively. At the start of configuration, memory circuit 30 provides preamble data to FPGA 37a via line 34, including a length count indicating how many bits of configuration data are going to be provided to FPGAs 37a-37c. This preamble data is stored in FPGA 37a, and passed on to FPGAs 37b and 37c via lines 76a and 76b, respectively. Thereafter, FPGA 37a receives configuration data from memory 30 via lead 34 and uses that data to configure itself, but holds its serial output lead 76a high. As soon as FPGA 37a is done configuring itself, FPGA 37a begins to pass the serial data from lead 34 to lead 76a. This data is then used by FPGA 37b to configure itself. While FPGA 37b is configuring itself, it holds serial output lead 76b high. As soon as FPGA 37b is done configuring itself, it begins to pass the serial data from lead 76a to lead 76b. FPGA 37c receives and uses the data from lead 76b to configure itself. Of importance, each FPGA 37a to 37c includes a counter which increments every time a clock signal is received on lead 35. When the number of counted clock signals equals the length count, then all of FPGAs 37a to 37c know that configuration is complete. Each FPGA 37a, 37b, 37c includes an associated open drain output line 38a, 38b, 38c which are "AND-tied" and coupled to memory circuit 30. When FPGAs 37a, 37b and 37c have counted a number of clock pulses equal to the length count, all of lines 38a, 38b and 38c are held active (e.g. high), which then causes memory circuit 30 to tri-state buffers 51 and 68 (FIG. 7a), and to cease sending configuration data to the FPGAs. While FIG. 8a shows three FPGAs, the same principle can be applied to any other number of FPGAs.

(Leeds, col. 6, lines 22 – 54)

As this portion of Leeds makes clear, what is being input from element 30 is a clock signal via lead 35 and preamble data via lead 34, it is not the output of an elementary block as claimed.

For these reasons, applicants respectfully submit that none of the pending claims is anticipated or rendered obvious by Leeds.

In view of the foregoing, it is respectfully asserted that the claims are now in condition for allowance.

Conclusion

It is believed that this Amendment places the above-identified patent application into condition for allowance. Early favorable consideration of this Amendment is earnestly solicited.

If, in the opinion of the Examiner, an interview would expedite the prosecution of this application, the Examiner is invited to call the undersigned attorney at the number indicated below.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case. Please charge any additional required fee or credit any overpayment not otherwise paid or credited to our deposit account No. 50-1698.

Respectfully submitted,

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Dated: August 6, 2007

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